

thereof is respectfully requested. Applicants respectfully submit that Claims 1-2 and 8-19 are patentable over Yamamoto, for reasons set forth in detail below.

Applicants' Claim 1 recites a data storage system including a first disk drive unit, a second disk drive unit, coupled to the first disk drive unit by a bus, a main cache memory, coupled to the bus, that caches data from at least one of the first disk drive unit and the second disk drive unit, and a secondary memory. The secondary memory is provided as part of the first disk drive unit, where the secondary memory has at least two sections, a first section used by the first disk drive unit to facilitate disk accesses and a second section used to cache data from the second disk drive unit.

Applicants' Claim 2 recites a disk drive unit, including an interface that communicates data to and from the disk drive unit; a disk platter that stores data; and a controller. The controller is coupled to the interface and the disk platter. The controller provides and accepts data signals that control the disk drive unit and communicate data therewith. The controller includes a memory having a portion that is useable as cache for data that is not stored on the disk platter.

Applicants' Claim 8 recites a data storage system including: a first disk drive including a section of onboard memory associated with the first disk drive, a second disk drive that provides data to the first disk drive, and memory for caching data of the data storage system. The memory includes the section of onboard memory associated with the first disk drive wherein the section includes a portion of data cached from at least the second disk drive. Claims 9-19 depend from Claim 8.

Yamamoto discloses dual writing of data through the effect of two controllers. (Col. 1, Lines 6-7). Yamamoto's Figure 1 illustrates a general configuration that includes a primary controller 104 connected to one or more disk units 105, a secondary controller 109 connected to one or more disk units 105, and one or more processing units 100 each including a CPU 101, a main storage 102 and a channel 103. The primary controller includes a control memory 107 and a cache memory 108 that are non-volatized. For enhancing reliability, each memory may be dualized. (Col. 3, Lines 38-50). The primary controller 104 provides a function to transfer data to the secondary controller 109. (Col. 1, Lines 56-58). The write data managing information 113 corresponding to the write data record 112 is created on the control memory 107. (Col. 3, Line 65-Col. 4, Line 5). The write data managing information 113 includes information indicating a logical disk number and a location on the logical disk number of where the write data is to be written, a pointer 123 to a location in the cache memory 108 of the corresponding write data 112, a numeral 124 denoting a necessity bit indicating that write data is required to be transferred to the secondary controller 109, and a secondary logical disk number 114 indicating the secondary logical disk paired for dual writing corresponding to the logical disk of the primary controller 104. The control memory 107 of the secondary disk controller 109 contains a primary logical disk number corresponding to the logical disk of the secondary controller 109 paired for dual writing. (Col. 4, Line 14-Col. 5, Line 6; Figure 2). The primary controller provides a primary write data receiving unit which is started when it receives the request for write 110. At first, the received write data 112 is stored in the cache memory 108. The write data receiving unit then operates to secure the

write data managing information 113 inside the control memory for processing the request. Completion of the write request is reported to the processing unit 100. The process of writing the data onto the disk is executed by the primary controller at a later stage. The primary controller then transmits the write data to the secondary controller 109 having a pair for dual writing located therein by referring to the corresponding secondary logical disk number 114 using a primary write data transmitting unit 140. The primary write data transmitting unit 140 waits for a report on the completion from the secondary controller 109. When a report is received, the necessity bit is set off and the next write data to be transmitted is found. The secondary controller 109 has a secondary write data receiving unit which is started when data is received from the primary controller 104 and operates likewise to that of the primary write data receiving unit except that the necessity bit 124 is not set. After the write data from the primary controller 104 is written to cache 108, the completion of the write is reported to the primary controller 104. (Col. 5, Lines 9-57). The secondary controller enables generation of a state of all write data records 113 on or before a reference time. This operation makes it possible for the secondary controller 109 to do a recovering process without leaving any intermediate result of a transaction if the primary controller 104 is broken. (Col. 6, Lines 7-16).

Applicants' Claim 1, is neither disclosed nor suggested by the Yamamoto, in that Yamamoto neither discloses nor suggests *a data storage system comprising a main cache memory that caches data from at least one of the first disk drive unit and the second disk drive unit, and a secondary memory, provided as part of the first disk drive unit, wherein the secondary memory has at least two sections, a first section used by*

the first disk drive unit to facilitate disk accesses and a second section used to cache data from the second disk drive unit, as set forth in Applicants' Claim 1. Yamamoto neither discloses nor suggests any memory of one drive unit being used to cache data for another drive unit, as set forth in Applicants' Claim 1. Although Yamamoto discloses a main storage 102, Yamamoto does not disclose the main storage 102 being used for caching any data. Furthermore, Yamamoto discloses a secondary controller 109 writing write data 112 transmitted from the primary controller 104 to the cache 108 included in the secondary controller where the secondary controller also includes a control memory 107. However, the cache 108 included in the secondary controller is not used as a cache for the primary controller. Rather, the cache 108 is used as a cache when performing writes to a disk connected to the *secondary* controller, not the *primary* controller. In addition, although a first device and cache memory of the primary controller and a second device and second cache of the secondary controller may contain the same data by being paired for dual writing, this arrangement neither discloses nor suggests using the cache memory of the secondary controller as a cache when performing operations to the first device.

For reasons similar to those set forth above regarding Claim 1, Applicants' Claim 2 is neither disclosed nor suggested by Yamamoto in that Yamamoto neither discloses nor suggests *a disk drive unit, comprising: a controller coupled to said interface and said disk platter, the controller providing and accepting data signals that control the disk drive unit and communicate data therewith, wherein said controller includes a*

memory having a portion that is useable as cache for data that is not stored on said disk platter, as set forth in Applicants' Claim 2.

For reasons similar to those set forth above regarding Claim 1, Applicants' Claim 8 is neither disclosed nor suggested by Yamamoto in that Yamamoto neither discloses nor suggests *a data storage system comprising: a first disk drive including a section of onboard memory associated with the first disk drive; memory for caching data of the data storage system, said memory including said section of onboard memory associated with said first disk drive wherein said section includes a portion of data cached from at least said second disk drive,* as set forth in Applicants' Claim 8.

In view of the foregoing, Applicants respectfully submits that Yamamoto neither discloses, teaches, or suggests Applicants' Claims 1-2 and 8-19 and requests that the rejection be reconsidered and withdrawn.

The rejection of Claims 3-7 and 20-31 under 35 U.S.C. 103(a) as being unpatentable over Yamamoto is hereby traversed and reconsideration thereof is respectfully requested. Claims 3-7 and 20-31 are patentable over Yamamoto.

Applicants' Claim 3 recites a data storage device including onboard volatile memory; and a section of onboard volatile memory associated with the data storage device and used as a cache including data cached from at least one other data storage device. Claims 4-7 depend from Claim 3.

Applicants' Claim 20, recites a method of caching data. Data is obtained from a first disk drive unit. At least a portion of the data is stored on volatile memory that is part of a second disk drive unit different from the first disk drive unit. Claims 21-25 depend from Claim 21.

Applicants' Claim 26, recites a computer program product for caching data including machine executable code for obtaining data from a first disk drive unit; and machine executable code for storing data on memory of a second disk drive unit different from the first disk drive unit. Claims 27-31 depend from Claim 26.

Yamamoto is summarized above.

For reasons similar to those set forth above regarding independent Claim 1, Applicants' Claim 3 is neither disclosed nor suggested by the Yamamoto in that the Yamamoto neither discloses nor suggests *a data storage device comprising: onboard volatile memory; and a section of onboard volatile memory associated with the data storage device and used as a cache including data cached from at least one other data storage device*, as set forth in Applicants' Claim 3.

For reasons similar to those set forth above regarding Applicants' Claim 1, Applicants' Claim 20 is neither disclosed nor suggested by Yamamoto in that the Yamamoto neither discloses nor suggests *a method of caching data, comprising: obtaining data from a first disk drive unit; and storing at least a portion of the data on*

volatile memory that is part of a second disk drive unit different from the first disk drive unit, as set forth in Applicants' Claim 20.

For reasons similar to those set forth above regarding Applicants' Claim 1, Applicants' Claim 26 is neither disclosed nor suggested by the Yamamoto in that Yamamoto neither discloses nor suggests *a computer program product for caching data, comprising: machine executable code for obtaining data from a first disk drive unit; and machine executable code for storing data on memory of a second disk drive unit different from the first disk drive unit*, as set forth in Applicants' Claim 26.

In view of the foregoing, Applicants respectfully submits that Yamamoto neither discloses, teaches, or suggests Applicants' Claims 3-7 and 20-31, and requests that the rejection be reconsidered and withdrawn.

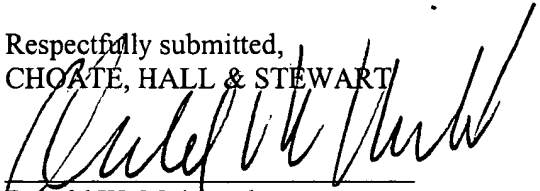
Based on the above, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

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Date

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Clean copy of claims as amended herein

19. (Once Amended) The data storage system of Claim 18, further comprising:
a command interpreter that interprets commands in connection with a data caching
operation of at least one of said section of onboard memory and said system cache
memory.